EMIF02-MIC03F2

2 LINE EMI FILTER AND ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS:

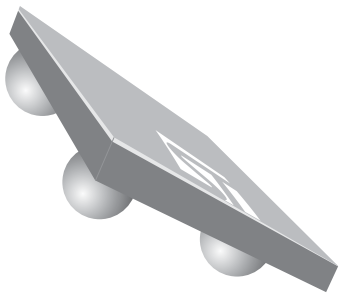
Where EMI filtering in ESD sensitive equipment is required :

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF02-MIC03 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 Flip-Chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up 15 kV.



Flip-Chip package

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.07 mm x 1.47 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging

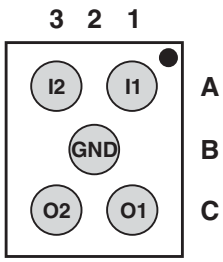
COMPLIES WITH THE FOLLOWING STANDARDS:

IEC 61000-4-2

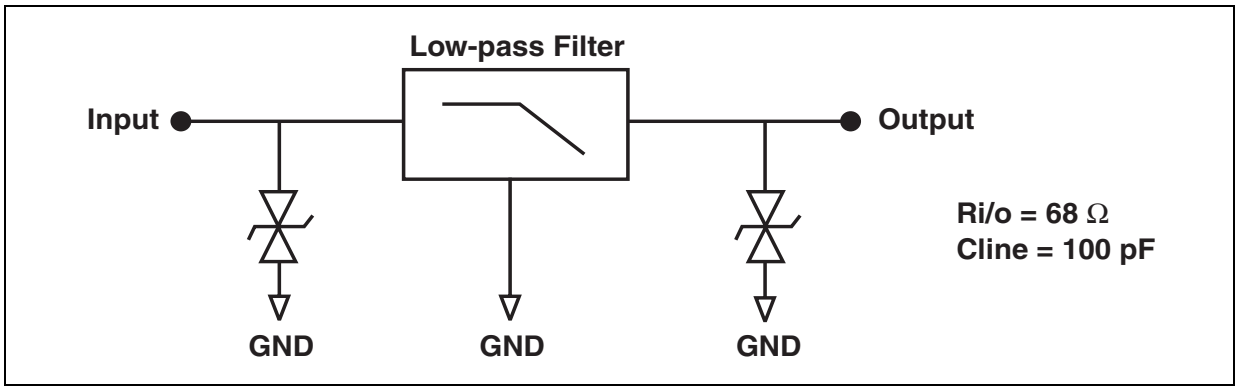
Level 4 on input pins 15 kV (air discharge)
8 kV (contact discharge)
Level 1 on output pins 2 kV (air discharge)
2 kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3

PIN CONFIGURATION (bump side)



BASIC CELL CONFIGURATION



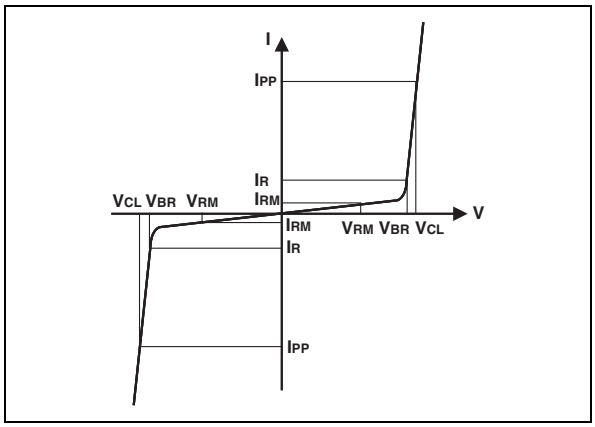
TM: IPAD is a trademark of STMicroelectronics.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to 150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8		V
I_{RM}	V_{RM} = 3 V per line			500	nA
$R_{I/O}$	Tolerance ± 20 %		68		Ω
C_{line}	V_R = 0 V		100		pF

Fig. 1: S21 (dB) attenuation measurements and Aplac simulation.

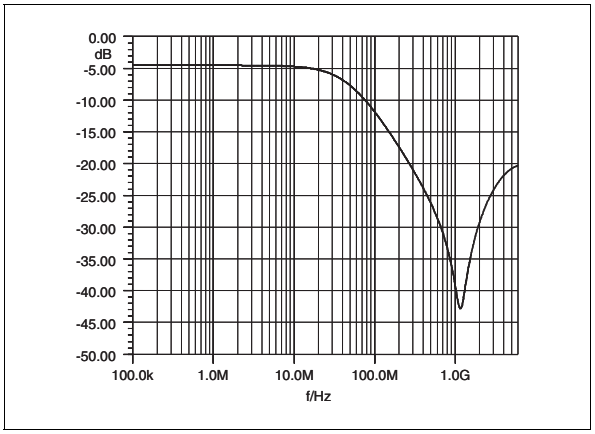


Fig. 2: Analog crosstalk measurements.

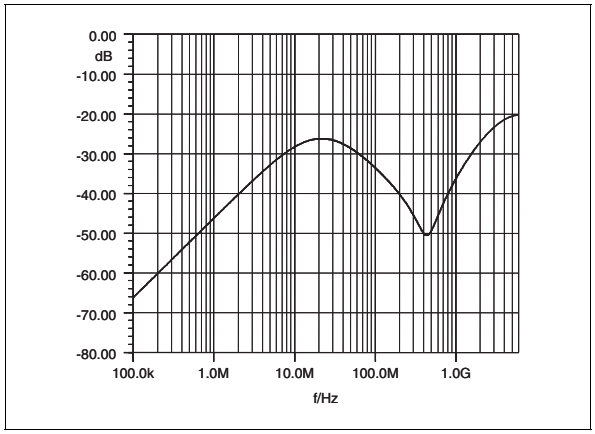


Fig. 3: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and one output V(out).

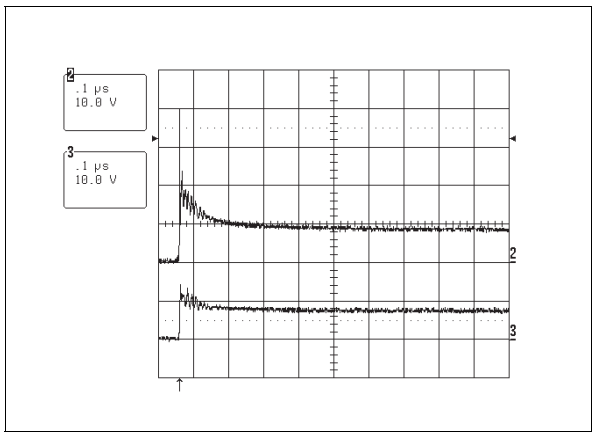


Fig. 4: ESD response to IEC61000-4-2 (–15kV air discharge) on one input V(in) and one output V(out).

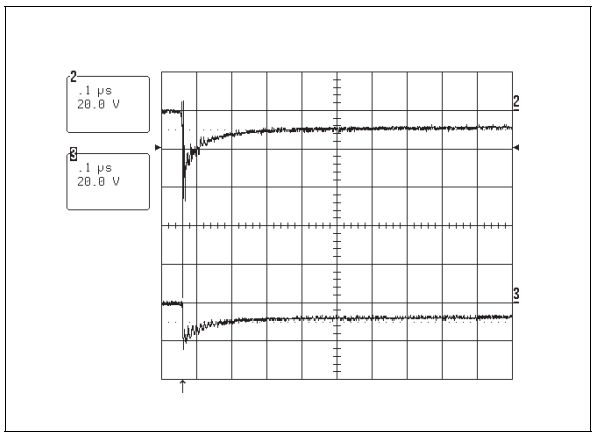
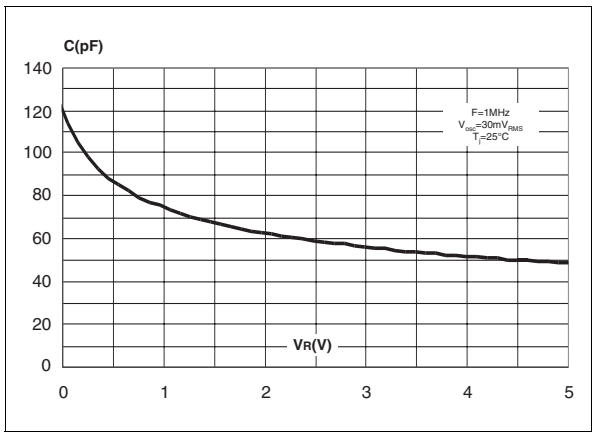
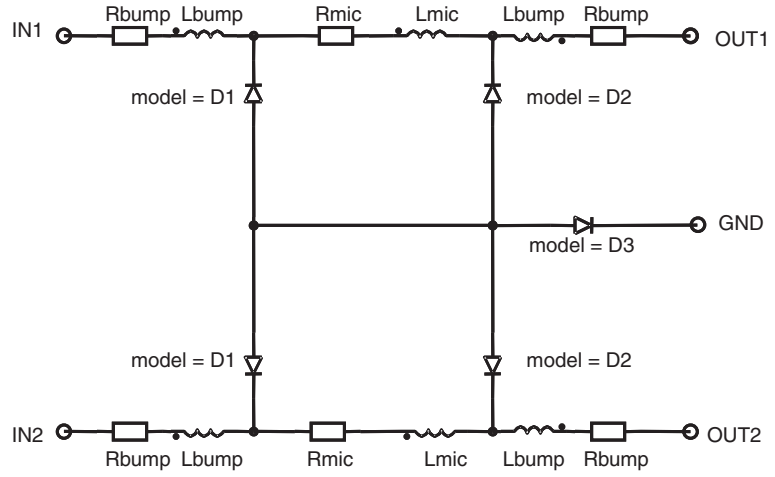


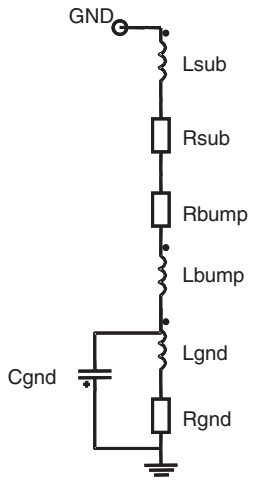
Fig. 5: Line capacitance versus applied voltage.



Aplac model



EMIF02-MIC03F1 model

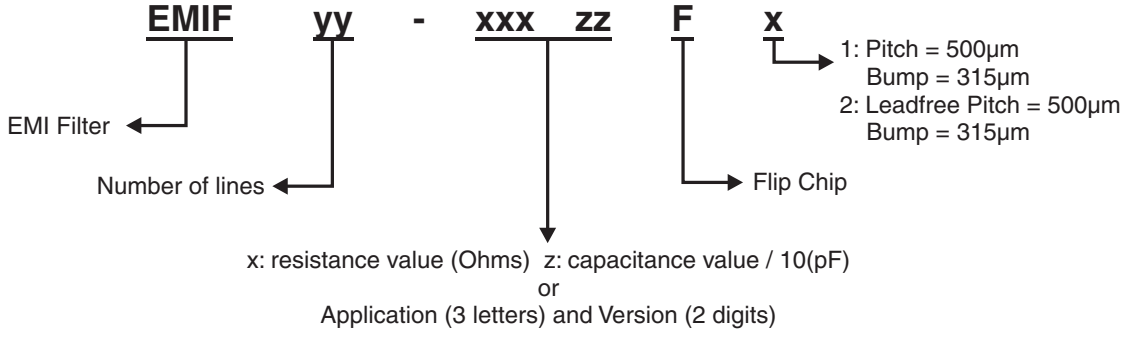


Ground return

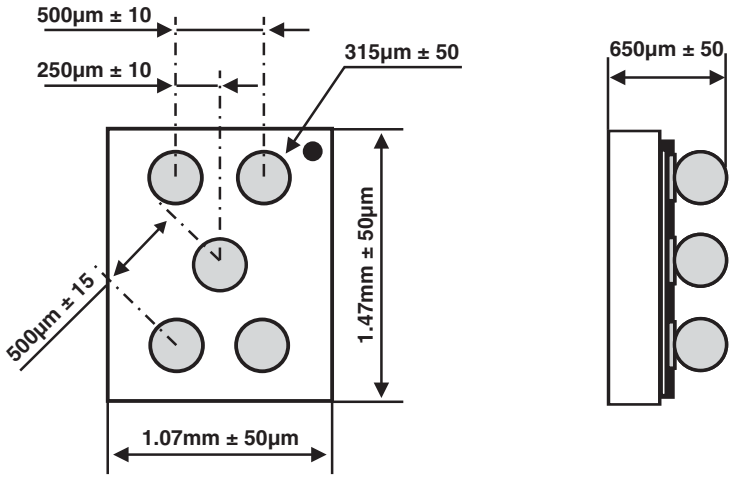
Aplac parameters

Model D1	Model D3	Model D2	aplacvar Rmic 68
CJO=Cdiode1	CJO=Cdiode3	CJO=Cdiode2	aplacvar Lmic 10p
BV=7	BV=7	BV=7	aplacvar Cdiode1 100pF
IBV=1u	IBV=1u	IBV=1u	aplacvar Cdiode2 3.6pF
IKF=1000	IKF=1000	IKF=1000	aplacvar Cdiode3 1.17nF
IS=10f	IS=10f	IS=10f	aplacvar Lbump 50pH
ISR=100p	ISR=100p	ISR=100p	aplacvar Rbump 20m
N=1	N=1	N=1	aplacvar Rsub 0.5m
M=0.3333	M=0.3333	M=0.3333	aplacvar Rgnd 10m
RS=0.7	RS=0.12	RS=0.3	aplacvar Lgnd 50pH
VJ=0.6	VJ=0.6	VJ=0.6	aplacvar Cgnd 0.15pF
TT=50n	TT=50n	TT=50n	aplacvar Lsub 10pH

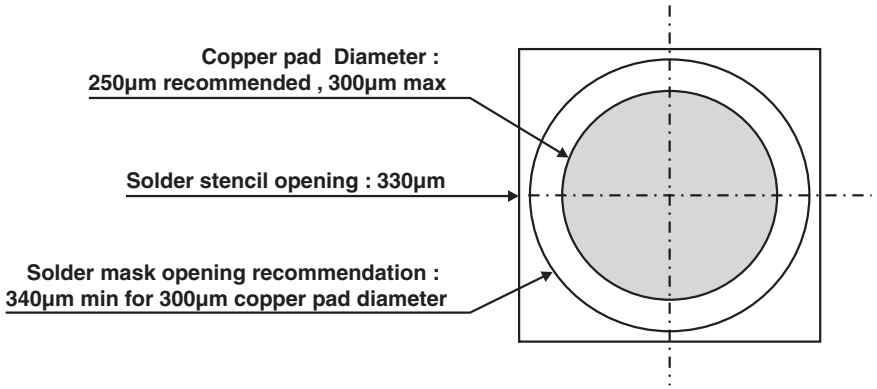
ORDER CODE


EMIF yy - xxx zz F x
EMI Filter
Number of lines
x: resistance value (Ohms) z: capacitance value / 10(pF)
or
Application (3 letters) and Version (2 digits)
Flip Chip
1: Pitch = 500µm
Bump = 315µm
2: Leadfree Pitch = 500µm
Bump = 315µm

PACKAGE MECHANICAL DATA
FLIP CHIP

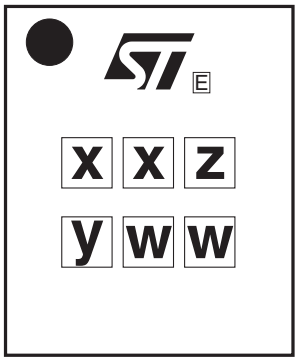


FOOT PRINT RECOMMENDATIONS

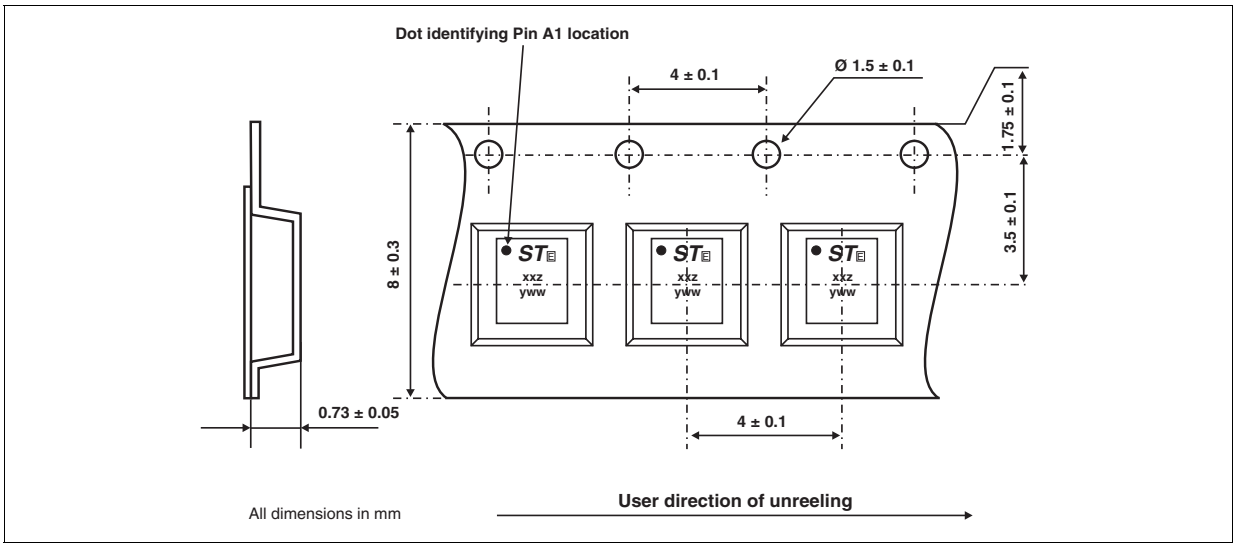

Copper pad Diameter :
250µm recommended , 300µm max
Solder stencil opening : 330µm
Solder mask opening recommendation :
340µm min for 300µm copper pad diameter

MARKING

Dot, ST logo
xx = marking
z = manufacturing location
yww = datecode
(y = year ww = week)



PACKING



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC03F2	FW	Flip-Chip	2.1 mg	5000	Tape & reel (7”)

Note: More packing informations are available in the application notes
AN1235: "Flip-Chip: Package description and recommendations for use''
AN1751: "EMI Filters: Recommendations and measurements"

REVISION HISTORY

Date	Revision	Changes
14-Oct-2005	1	Initial release.

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